HIGH PERFORMANCE WIDE-BAND & MEDIUM-BAND POWER AMPLIFIER MMICS⌖

T. Apel, R. Bhatia◆, and B. Lauterwasser✧

Teledyne Electronic Technologies
MicroSystems Products
1274 Terra Bella Avenue
Mountain View, CA 94043
FAX: (415) 968-6533

ABSTRACT

Recent MMIC technology advancements, both in PHEMT devices and in new integrated power circuit techniques, allow pace setting power amplifier performance to be achieved. This combination has been key to realizing the full cost/performance inherent in MMIC power technology.

This paper describes two advanced MMIC power amplifiers covering the 6-18 GHz and 8-14.5 GHz bands. Both chips are based on a novel two section distributed amplifier structure that employs bandpass networks instead of the conventional lowpass image-parameter networks. A new matrix amplifier structure is also used in the first stage of the 8-14.5 GHz PA. Bias networks are fully integrated to allow automated assembly. Significant milestones in wideband power and efficiency have been achieved.

INTRODUCTION

Broadband power chips have been a subject of interest for some time [1,2,3,4, and 5]. Previous efforts have simultaneously yielded respectable power and efficiency but too often have been reported for only one or two stages. When comparing efficiency results it is important to consider overall gain. Practical attention to integration of bias circuitry and impedance transforming circuitry is also important. Platzker, et al[6], have done well in setting the pace to date with a four stage high performance PA with integrated bias networks and 50 Ω ports.

To provide systems acceptance, the challenge is to simultaneously provide superior gain, power, and efficiency performance within an affordable chip area. The two chips presented here offer significant improvements in power, gain, and efficiency. Affordability also requires integrated bias circuitry for low cost assemblies. Goals in the TMM9205 (wide-band PA) and TMM9206 (medium-band PA) developments were targeted to meeting these requirements. The results presented in this paper are first design pass.

It is well known that distributed amplifiers offer lower sensitivity to process variation[2] than lossy compensated multistage amplifiers. Other advantages include higher input and interstage impedances, and lower $|S_{21}|$ ripple. Historically, distributed amplifier approaches have **not** resulted in *state-of-the-art* performance. Conventional distributed approaches are suboptimal power amplifiers for the following reasons:

❶ A uniform impedance drain network cannot provide uniform loading to the array of active devices. Optimum loading can only be provided to one device, at best.
❷ The internal drain network termination absorbs significant power at lower frequencies.
❸ Losses in the gates and gate network result in diminishing drive to successive devices.
❹ Drain bias choke inductors in the form of rectangular spirals contribute additional loss, usually resonate in-band, and are not capable of passing the current levels required for a high power final stage.

Clearly, If pace setting power performance is to be achieved with the benefits offered by distributed amplification these limitations must be overcome. The resultant distributed amplifier approach, presented here, is unconventional. The TMM9205 AND TMM9206 chips, shown in Figures 1 and 2, are examples of distributed power amplifiers in which the conventional distributed amplifier limitations have been overcome. Topologically, the TMM9205 has two identical channels, each of which are comprised of three stages of distributed amplification. The TMM9206 is a single channel amplifier comprised of four stages of distributed amplification. The driver and final stages are similar to those of the TMM9205; however, the first two stages are realized in a novel matrix configuration. Single gate PHEMTS serve as the active device in each stage. Impedance matching is provided between stages since distributed amplifier stages are loaded for power performance.

Both linear and non-linear design simulations were performed. The linear simulation also provided a quasi-linear analysis of the loading at each power device. This is necessary as well as more difficult in a distributed power amplifier, due to the phase staggered loading.

⌖ This work was supported by the Raytheon/Texas Instrument Joint Venture as part of the MIMIC Phase-II Program, NAVAIR Contract N00019-91-C-0210.

◆ R. Bhatia is presently with Hughes Network Systems., San Diego, CA.

✧ B. Lautowasser is with Raytheon ADC-MMC., Andover, MA.

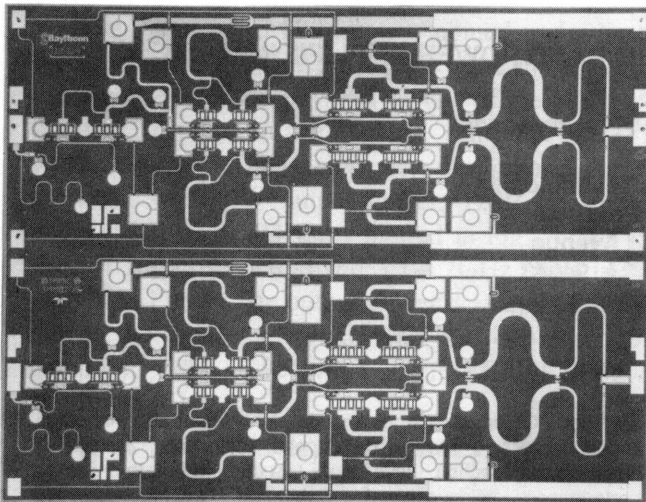

Fig. 1 TMM9205 Wide-Band Power Amplifier.

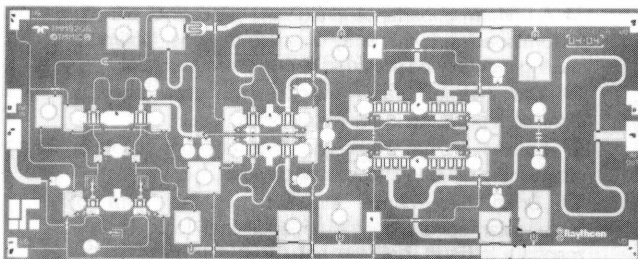

Fig. 2 TMM9206 Medium-Band PA Driver.

The TMM9205 chip is 6.5mm x 5.1mm, and the TMM9206 is 6.4mm x 2.5mm. The power PHEMT process, which is described in the next section, includes via holes and TaN thin film GaAs resistors. Gates were written with E-beam lithography. Both amplifiers operate from a single positive supply (V_{dd} = +8v), and a negative supply (V_{gg} = -0.3v). The quiescent operating current is nominally 650 mA / amplifier channel. Compact bias distribution networks are fully integrated. The only external components required are a single capacitor per bias line.

PROCESS DESCRIPTION

Raytheon's quarter micron power PHEMT foundry process utilizes double pulse-doped pseudomorphic HEMT material grown by molecular beam epitaxy and supplied by commercial vendors of epitaxial wafers. The layer structure is similar to that described by Shanfield, et. al.[7]. An N+ cap layer is used for low resistance ohmic contacts while a ten period superlattice is incorporated into the buffer layer to enhance electron confinement in the InGaAs channel. The fabrication sequence is nearly identical to that used for Raytheon's MESFET-based MMICs and has been described by Danzilio, et.al. [8]. A double recess geometry is used to improve breakdown voltage (typically 12-14 volts). The quarter micron T-gate is defined using a bilayer resist process in which the stem is exposed in a thin layer of resist for high resolution while the cap is exposed independently in a second resist layer to provide good control of gate resistance. Thin film resistors are formed using reactively sputtered tantalum nitride, which produces a consistent sheet resistance of 6Ω/□ with low temperature coefficient of resistance. Capacitors are standard MIM type with silicon nitride serving as both the capacitor dielectric and the device passivation film.

Raytheon's Monolithic Microwave Center (MMC) foundry has for the past two years, used a reticle based PCM approach for process control instead of the more common "drop-in" approach used by many GaAs foundries. The use of a PCM "Coupon" in every reticle allows for a direct site by site correlation between MMIC performance and in-process DC parametric data. With typically 50-100 test sites per wafer, reliable statistics on process uniformity and repeatability are readily obtained. Typical values of DC device parameters for the quarter micron power PHEMT process are: maximum open channel current (Imax) 550 mA/mm, peak transconductance 375 mS/mm, Idss 265 mA/mm, pinch-off voltage -0.9 volts, and gate to drain reverse breakdown voltage -13 volts.

Device RF Performance

The combination of PHEMT material characteristics and quarter micron T-gate geometry produces outstanding device RF performance through Ku-band. Figure 3 illustrates the RF performance of a single 1.2mm device at 18 GHz over a range of gate bias from -1.0v to 0.0v. Maximum gain increases from 7 dB (class B) to 9 dB (class A) with output power increasing by 1 dBm at peak efficiency. The trade-off for higher gain and power is a reduction in power added efficiency from 53% to 46%. This data represents performance from the upper end of the device performance distribution; however, the more critical issues are the performance level of a typical device and the range in performance to be expected from the process (or equivalently, the repeatability of device performance from wafer lot to wafer lot). Figure 4 shows histograms of 18 GHz RF performance for a population of 241 identical 1.2 mm PHEMT devices which span a total of 11 wafer lots processed over a period of approximately 18 months. The median values for these distributions are 28.5 dBm output power, 6.2 dB associated gain, and 46.2% power added efficiency. Each of the distributions is well behaved and reasonably tight, thus providing a high level of confidence for the circuit designer in the RF performance of devices used in the MMIC.

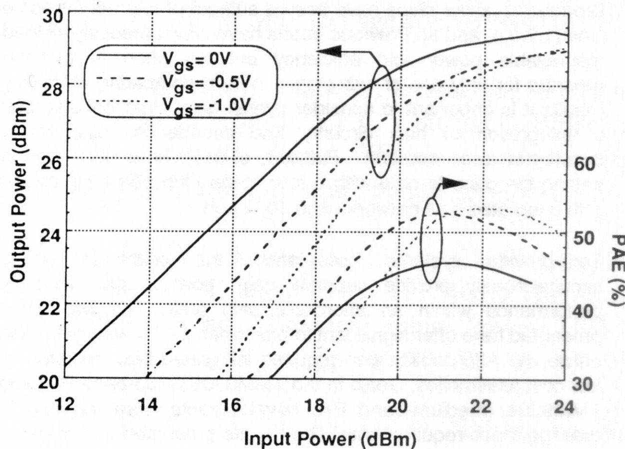

Fig. 3 Power PHEMT Device at 18 GHz, Wg=1.2mm.

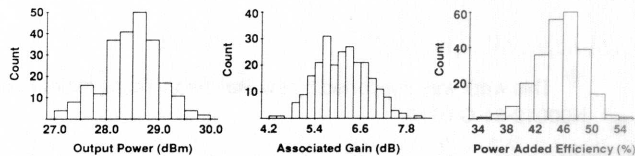

Fig. 4 RF Performance Distribution from Population of 241 PHEMT Devices over 11 Process Lots (18GHz, Vds=7v).

RF DESIGN

All stages of both PA chips are realized as two section distributed amplifiers. The reasons for this unorthodox approach will be discussed shortly. The total gate width in the three stage PA channel is 6664 µm. A 1224 µm input stage drives a 2040 µm second stage, followed by a 3400 µm final output stage. The four stage medium-band PA has a total gate width of 6448 µm. The matrix first stage is comprised of a pair of 224 µm devices driving a pair of 450 µm devices. The driver and final amplifier stages are 1700 µm and 3400 µm, respectively.

Distributed Approach Tradeoffs

In order to better understand the rationale for the two section distributed power amplifier (DPA) approach, it is useful to recognize the conventional in-phase combined, lossy compensated designs as the limiting case (N=1) of general DPA (N >1). Table 1 illustrates many of the key performance tradeoffs related to the number of distributed sections (N). The conventional N=1 case offers better load uniformity and power loading than a conventional distributed amplifier with large N. Alternatively, The conventional DA with large N is less sensitive to process and device changes, offers higher impedances and lower gain ripple. It is important to recognize that the N=2 case offers the *best of both worlds*, by balancing the desired behavior against the undesired attributes of the two extremes. The active device in any power amplifier stage is comprised of many smaller constituents. This is especially true of high power final amplifier stages. Power performance is dependent on optimum device loading. Since the constituent devices within a power stage may not be loaded uniformly, **both** nominal impedance level and load uniformity must be considered.

TABLE 1 Distributed PA Topology Trade-Off

PARAMETER	N=1 (IN-PHASE)	N=2	N ≥ 5
Response Sensitivity	Poor	Good	Very Good
Power Load Uniformity	Excellent	Very Good	Poor
Output Impedance Level	Low Z	Low Z	Moderate High
Achievable Power Load	Very Good	Good to Very Good	Poor
Input Impedance Level	Low Z	Moderate Z	High Z
Small-Sig. $|S_{22}|$	Poor	Poor	Very Good
Small-Sig. $|S_{21}|$	Low	Satisfactory	Good
Small-Sig. $|S_{21}|$ Ripple	High	Satisfactory	Low

As indicated in Table 1, conventional in-phase PAs can be superior in terms of load uniformity. It is well known that conventional DAs provide increasing FET load impedances as the output end of the drain line is approached. If the impedance of the drain line is lowered to minimize the error VSWR from the optimum power load, the resultant error is still not acceptable for large N. This can be seen in Figure 5. Tapered line[2,3,9,10 and 11] approaches have offered some power loading improvement in lowpass DAs. The approach taken here goes beyond simply tapering the drain line. By employing only two distributed sections the natural loading disparity is minimized to the greatest extent possible. Secondly, the use of bandpass drain networks allows an additional degree of freedom in impedance transformation.

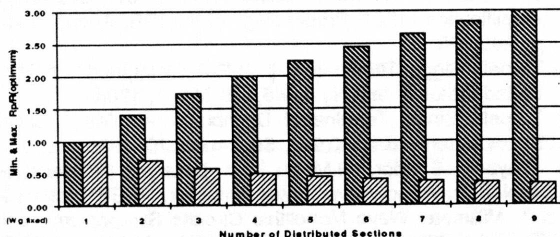

Fig. 5 FET Load Extrema (Relative Optimum = 1.0)

One of the most difficult aspects of a conventional FET power amplifier design is absorbing the relatively high input Q of the device. This is important for input and interstage matching network design. Broadband interstage networks are especially challenging due additionally to the required transformation. Distributed amplifiers offer an N-fold advantage in input impedance level, for N distributed sections. Even a two section DA has a 2:1 impedance advantage over a conventional in-phase design.

Another power limitation present in conventional distributed amplifiers is the loss of drive to FETs near the load end of the gate line, due to gate resistance at previous FETs. It is well known that drive can be tapered by the use of series capacitors [2,12] at each gate or by the use of series M-derived gate lines. The designs presented here uses series gate capacitors.

Bandpass Drain Line

The internal drain termination has been eliminated in the singly terminated bandpass 3-port network shown in Figure 6. Ports 1 and 2 provide the FET interfaces. The output is obtained from port-3. The coupling between the two resonators is controlled primarily by the common grounded inductor. It can also be seen from Figure 6 that the impedance transformation between ports 1 and 2 can be easily set over a wide range while maintaining the same resonant frequency; hence, line impedance tapering is readily available.

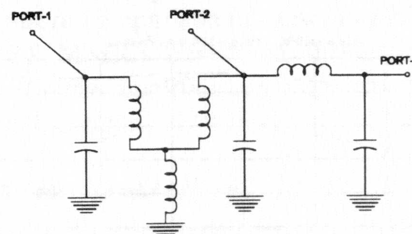

Fig. 6 Bandpass Distributed Drain Line.

Perhaps the most important feature of the bandpass distributed drain line is the DC feed path. Conventional distributed amplifiers with lowpass drain lines require a large shunt *"choke"* inductor through which drain bias is provided. Practical limitations in self-resonance and conductor width, due to current density, have not allowed previous wideband distributed power amplifiers to operate at levels much greater than +27 dBm. The bandpass drain network provides a natural means of feeding drain bias to the FETs without a large shunt choke inductor, since all three inductors are relatively small tuning elements.

MEASURED PERFORMANCE

A summary of chip RF performance is shown in Figures 7 through 11. These are significant first pass test results.

Typical small signal gain is +20 dB from The WB-PA (TMM9205) and +30 dB from the MB-PA (TMM9206). The WB-PA power performance is typically +34dBm at -2dB compression and the saturated power is +35 dBm. The typical MB-PA -2dB compression power is 32 dBm. Input and output return loss are typically better than -10 dB. Typical noise figure ranges from 4.5 dB at midband to 5.8 dB at the corner frequencies..

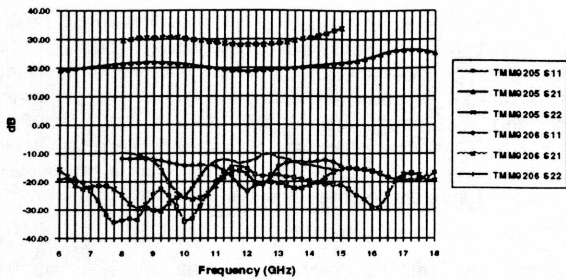

Fig. 7 Small Signal Response of TMM9205 and TMM9206.

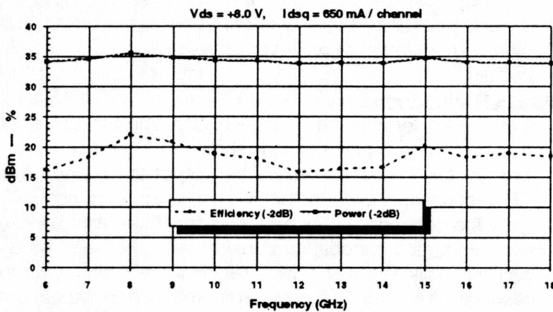

Fig. 8 Power and Efficiency of TMM9205.

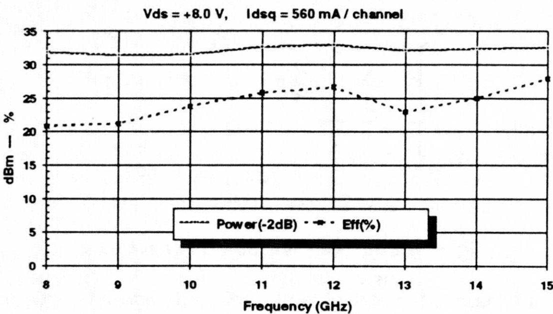

Fig. 9 Power and Efficiency of TMM9206.

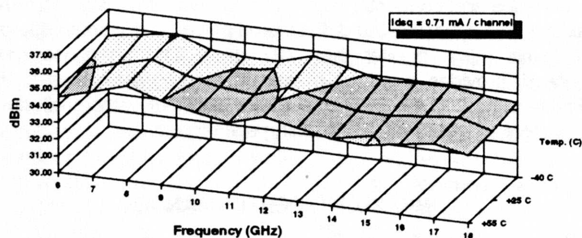

Fig. 10 Power vs Temperature of TMM9205.

CONCLUSIONS

The reported level of broadband power performance in the C-X-Ku range is a significant advance in single chip performance. Both chips presented contain integrated bias networks. The demonstrated chip performance highlights the major developments in broadband power design technology and foundry process during the past few years, in extending performance capability and repeatability of complex MMIC Circuits.

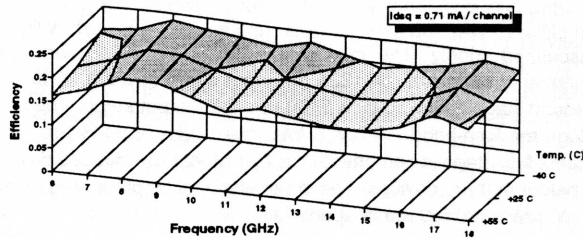

Fig. 11 Efficiency vs Temperature of TMM9205.

ACKNOWLEDGMENT

This work was made possible through the Raytheon/TI Joint Venture as part of the MIMIC Phase-II Program. We gratefully acknowledge the efforts of R. Shumovich, C. Bunszel and H. Renaud (Raytheon) who provided a very smooth interface with the Raytheon foundry. A. Sanchez was key in much of the data gathering. Thanks also to Dr. Stephen Ludvik of Teledyne, who has been very supportive of the work and George Jerinic of Raytheon whose farsightedness provided the opportunity to do this work.

REFERENCES

[1] Y.Ayasli, L.Reynolds, R.Mozzi and L.Hanes, "2-20 GHz GaAs Traveling-Wave Power Amplifier," IEEE Transactions on MTT, Vol. 32, March 1984, pp.290-295.

[2] R.Halladay, M.Jones and S.Nelson, "A Producible 2 to 20 GHz Monolithic Power Amplifier," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Tech. Dig., June 1987, pp. 19-21.

[3] P.Dueme, G.Aperce and S.Lazar, "Advanced Design for Wideband MMIC Power Amplifiers," IEEE GaAs IC Symposium Tech. Dig., October 1990, pp.121-124.

[4] M.Oda, "A Stable GaAs 6-20 GHz High Gain and Power TWA," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Tech. Dig., June 1991, pp. 437-440.

[5] K.Johnson, A.Lum, S.Nelson, E.Reese and K.Saltzman, "High Efficiency Broadband Power Amplifier MMIC," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Tech. Dig., June 1992, pp. 43-45.

[6] A.Platzker, K.Hetzler and J.B.Cole, "Highly Dense Dual-Channel C-X-Ku and 6-18GHz MMIC Power Amplifiers," IEEE GaAs IC Symposium Tech. Dig., October 1991, pp. 339-342.

[7] S. Shanfield, A. Platzker, L. Aucoin, T. Kazior, B. Patel, A.Bertrand, W. Hoke, P. Lyman, "One Watt, Very High Efficiency 10 and 18 GHz Pseudomorphic HEMTs Fabricated by Dry First Recess Etching", IEEE MTT-S Digest, June 1-5, 1992, Albuquerque, NM, p. 639.

[8] D. Danzilio, P. White, L.K. Hanes, B. Lauterwasser, B. Ostrowski, F. Rose, "A High Efficiency 0.25 um Pseudomorphic HEMT Power Process," IEEE GaAs IC Symposium Tech. Dig., October 1992.

[9] E.Ginzton, W.Hewlett, J.Jasberg and J.Noe, "Distributed Amplification," IEEE Proceedings of the IRE, August 1948, pp.290-295.

[10] T.Apel, "Singly Terminated Push-Pull Distributed Amplifier" United States Patent No.4,446,445, May 1, 1984.

[11] T.Apel, "Singly Terminated Distributed Amplifier," United States Patent No.4,540,954, September 10, 1985.

[12] Y.Ayasli, S.Miller, R.Mozzi and L.Hanes, "Capacitively Coupled Traveling-Wave Power Amplifier," IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Tech. Dig., June 1984, pp. 52-54.